

Vishay High Power Products

ADD-A-PAK Generation VII Power Modules Schottky Rectifier, 100 A



PRODUCT SUMMARY			
I _{F(AV)}	100 A		

MECHANICAL DESCRIPTION

The ADD-A-PAK generation VII, new generation of ADD-A-PAK module, combines the excellent thermal performances obtained by the usage of exposed direct bonded copper substrate, with advanced compact simple package solution and simplified internal structure with minimized number of interfaces.

FEATURES

- 175 °C T_J operation
- Low forward voltage drop
- High frequency operation
- · Low thermal resistance
- UL pending
- Compliant to RoHS directive 2002/95/EC
- Designed and qualified for industrial level

BENEFITS

- Excellent thermal performances obtained by the usage of exposed direct bonded copper substrate
- High surge capability
- · Easy mounting on heatsink

ELECTRICAL DESCRIPTION

The VSKDS203.. Schottky rectifier doubler module has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature.

Typical applications are in high current switching power supplies, plating power supplies, UPS systems, converters, freewheeling diodes, welding, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS					
SYMBOL	CHARACTERISTICS	VALUES	UNITS		
I _{F(AV)}	Rectangular waveform	100	A		
V _{RRM}		100	V		
I _{FSM}	t _p = 5 μs sine	12 800	A		
V _F	100 Apk, T _J = 125 °C	0.87	V		
T _J	Range	- 55 to 175	°C		

VOLTAGE RATINGS				
PARAMETER	SYMBOL	VSKDS203/100	UNITS	
Maximum DC reverse voltage	V_{R}	100	V	
Maximum working peak reverse voltage	V_{RWM}	100	V	

Document Number: 93225 Revision: 04-May-10

VSKDS203/100

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ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current per leg	I _{F(AV)}	50 % duty cycle at T _C = 121 °C, rectangular waveform		100	
Maximum peak one cycle non-repetitive surge current	I _{FSM}	5 µs sine or 3 µs rect. pulse	Following any rated load condition and with rated V _{RRM} applied	12 800	Α
		10 ms sine or 6 ms rect. pulse		1700	
Non-repetitive avalanche energy	E _{AS}	T _J = 25 °C, I _{AS} = 5.5 A, L = 1 mH		15	mJ
Repetitive avalanche current	I _{AR}	Current decaying linearly to zero in 1 μ s Frequency limited by T _J maximum V _A = 1.5 x V _R typical		Α	

ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop	V _{FM}	100 A	T _J = 25 °C	0.99	V
		200 A		1.34	
		100 A	T _J = 125 °C	0.87	
		200 A		1.09	
Maximum reverse leakage current	I _{RM}	T _J = 25 °C	V _R = Rated V _R	3	A
		T _J = 125 °C		65	mA
Maximum junction capacitance	C _T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz), 25 °C		2750	pF
Typical series inductance	L _S	Measured lead to lead 5 mm from package body		7.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs
Maximum RMS insulation voltage	V _{INS}	50 Hz		3000 (1 min) 3600 (1 s)	V

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction and storage temperature range)	T _J , T _{Stg}		- 55 to 175	°C	
Maximum thermal resistance, junction to case per leg		R_{thJC}	DC operation	0.52	°C/W	
Typical thermal resistance, case to heatsink per module		R _{thCS}		0.1]	
Approximate weight				75	g	
Approximate weight				2.7	oz.	
Mounting torque ± 10 %	to heatsink		A mounting compound is recommended and the torque should be rechecked after a period of 3 h to allow for the	4	Nm	
	busbar		spread of the compound.	3	INIII	
Case style			JEDEC	TO-240AA co	mpatible	



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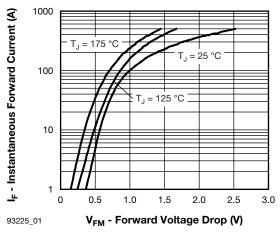


Fig. 1 - Maximum Forward Voltage Drop Characteristics

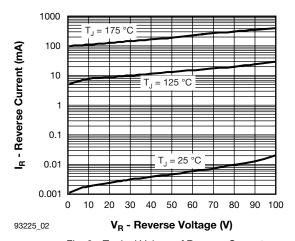


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

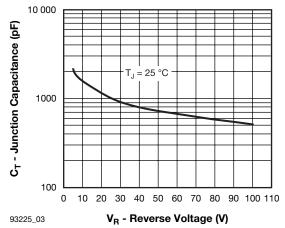


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

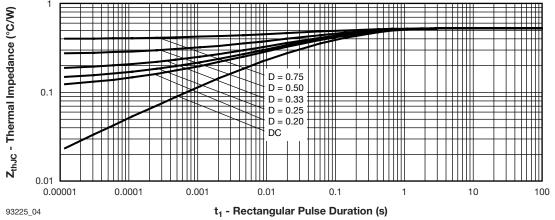


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

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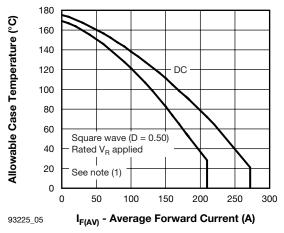


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current

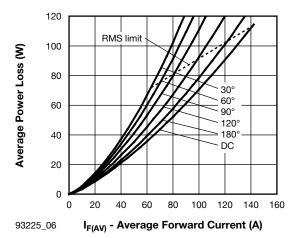


Fig. 6 - Forward Power Loss Characteristics

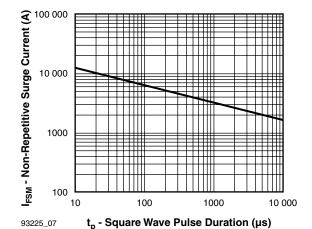


Fig. 7 - Maximum Non-Repetitive Surge Current

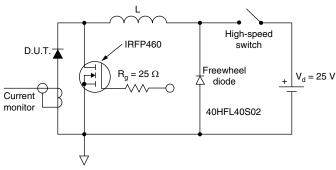


Fig. 8 - Unclamped Inductive Test Circuit

Note

 $^{(1)}$ Formula used: T_C = T_J - (Pd + Pd_{REV}) x R_{thJC}; Pd = Forward power loss = I_{F(AV)} x V_{FM} at (I_{F(AV)}/D) (see fig. 6); Pd_{REV} = Inverse power loss = V_{R1} x I_R (1 - D); I_R at V_{R1} = 80 % rated V_R

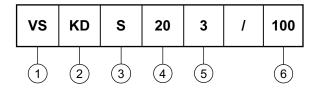


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ORDERING INFORMATION TABLE

Device code



1 - Vishay HPP

Circuit configuration:

KD = ADD-A-PAK - 2 diodes in series

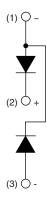
3 - S = Schottky diode

- Average current rating (20 = 200 A)

Product silicon identification

6 - Voltage rating (100 = 100 V)

CIRCUIT CONFIGURATION



LINKS TO RELATED DOCUMENTS			
Dimensions	www.vishay.com/doc?95369		



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Revision: 18-Jul-08

Document Number: 91000 www.vishay.com